CLAIMS

1. A semiconductor memory device, comprising a memory cell including first and second inverter circuits connected in loop to form first and second data storage nodes, and further comprising storage control means serially connected to a drive transistor of the second inverter circuit.

2. A semiconductor memory device according to claim 1, wherein the memory cell further comprises first and second access means for accessing the first and second data storage nodes, respectively, wherein the first access means is activated with a read signal thereby performing data transfer between a read bit line and the first data storage node, and the second access means is activated with a write signal thereby performing data transfer between a write bit line and the second data storage node.

3. A semiconductor memory device according to claim 1, wherein the memory cell further comprises first and second access means for accessing the first and second data storage nodes, respectively, wherein the first access means is activated with a read signal thereby performing data transfer between a read bit line and the first data storage node, and the second access means is activated with a write signal thereby resetting the second data storage node.

4. A semiconductor memory device according to claims 2 or 3, wherein the first and second inverter circuits forming the memory cell comprises a CMOS inverter circuit and the first and second access means and the storage control means comprises NMOS transistors, respectively.

5. A semiconductor memory device, comprising a sense amplifier including a bit line for performing data transfer to and from a memory cell, a data line for performing data transfer to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the data line, and data write means activated by a write

signal for transferring data from the data line to the bit line.

6. A semiconductor memory device according to claim 5, wherein the sense amplifier further comprises precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line.

7. A semiconductor memory device according to claim 6, wherein the data line of the sense amplifier comprises a read data line connected to the read means, and a write data line connected to the write means.

8. A semiconductor memory device according to claim 6, wherein the sense amplifier further comprises write precharge means connected to a write bit line, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

9. A semiconductor memory device according to claim 7, wherein the sense amplifier further comprises write precharge means connected to a write bit line, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

10. A semiconductor memory device according to claim 6, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

11. A semiconductor memory device according to claim 7, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

12. A semiconductor memory device according to claim 7, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and a write transistor having a gate input applied with a signal from the write data line, a source connected to a ground potential and a drain

connected to the write bit line.

13. A semiconductor memory device according to claim 6, wherein the sense amplifier further comprises a write bit line connected to an inverted write data line.

14. A semiconductor memory device according to claim 7, wherein the sense amplifier further comprises a write bit line connected to an inverted write data line.

15. A semiconductor memory device comprising a sense amplifier including a bit line and a write bit line for transferring data to and from a memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, data write means activated by a write signal for transferring data from the inverted write data line to the write bit line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line.

16. A semiconductor memory device comprising a sense amplifier including a bit line and a write bit line for transferring data to and from a memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line, wherein the write bit line is directly connected to the inverted write data line.

17. A semiconductor memory device comprising a sub word driver selecting a read word line in response to a main word signal, a read block selection signal and an inverted read block selection signal and selecting a write word line in response to the main word signal, a write block selection signal and an

inverted write block selection signal.

18. A semiconductor memory device according to claim 17, wherein the sub word driver comprises a first inverter circuit having an input applied with the main word signal for outputting a read word line signal, and a first transistor having a drain applied with the read word line signal, the first inverter circuit being formed between the read block selection signal and a ground potential, and the first transistor having a gate applied with the inverted read block selection and a source connected to the ground potential.

19. A semiconductor memory device according to claim 17, wherein the sub word driver comprises a second inverter circuit having an input applied with the main word signal for outputting a write word line signal, and a second transistor having a drain applied with the write word line signal, the second inverter circuit being formed between the write block selection signal and a ground potential, and the second transistor having a gate applied with the inverted write block signal and a source connected to the ground potential.

20. A semiconductor memory device comprising elements forming a memory cell placed in layout within an L-shaped region.

21. A semiconductor memory device according to claim 20, wherein the memory cell has an N well region having both sides formed with P well regions, and the N well region and the P well regions have one sides continuous with each other while sides opposite to the continuous sides are discontinuous thereby forming the L-shaped region in which one of the P well regions protrudes.

22. A semiconductor memory device according to claim 21, wherein a ground potential is extracted from a side of the P well region with a low height and a power supply voltage is extracted from the N well region in an area contiguous to the side.

23. A semiconductor memory device comprising a memory cell array, including disposed memory cells inverted in mirror in three directions, respectively,

which includes a central area having a vacant space in which elements forming the memory cells are not disposed.

24. A semiconductor memory device according to claim 23, wherein the vacant space has a layout in which elements forming a sense amplifier are placed.

25. A semiconductor memory device according to claim 24, wherein the sense amplifier comprises an inverter circuit and a read transistor for transferring a cell data from a bit line to a data line during read operation, and a write transistor for transferring data from a data line to the bit line during write operation.

26. A semiconductor memory device according to claim 24, wherein the sense amplifier includes elements placed in layout in a vacant space of an adjacent memory cell region.

27. A semiconductor memory device according to claim 26, wherein wiring of the sense amplifier are placed in layout in the adjacent memory cell region.

28. A semiconductor memory device according to claim 27, wherein the wiring of the sense amplifier are placed in layout in a part of a power wiring area of the adjacent memory cell region.

29. A semiconductor memory device according to claim 24, wherein a placement layout is such that one piece of the sense amplifier is placed in layout for an N-piece (with N representing a multiple of 8) of the memory cell.

30. A method of performing a reading in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means for accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when a read word line of the memory cell is activated, the storage control means turns off a driver transistor of the second inverter circuit and the first access means allows a bit line and the first data storage node to be connected to each

other for reading a memory cell data on a bit line.

31. A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means for accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when read and write word lines of the memory cell are activated, the storage control means turns off a drive transistor of the second inverter circuit to allow the second access means to reset the second data storage node to a low voltage potential and the first access means to connect a bit line and the first data storage node to each other, and subsequently, the write word line is inactivated to write data of the bit line to the first data storage node.

32. A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means for accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when read and write word lines of the memory cell are activated, the storage control means turns off the drive transistor of the second inverter circuit and the first access means allows a bit line and the first data storage node to be connected to each other to write data of a bit line to the first data storage node; while the second access means allows the write bit line and the second data storage node to be connected to each other to write data of the write bit line to the second data storage node.

33. A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop

to form first and second data storage nodes, first and second access means for accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

the storage control means turns off the drive transistor of the second inverter circuit during a write operation for the memory cell and the second access means allows a write bit line and the second data storage node to be connected to each other to write data of the write bit line to the second data storage node.

34. A semiconductor memory device according to claim 1, further comprising a sense amplifier including a bit line for transferring data to and from the memory cell, a data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the data line, and data write means activated by a write signal for transferring data from the data line to the bit line.

35. A semiconductor memory device according to claim 3, further comprising a sense amplifier including a data line connected to the read bit line and transferring data to and from an input and output circuit, an inverter circuit having an input applied with the read bit line, data read means for transferring an output of the inverter circuit to the data line, and data write means activated by the write signal for transferring data from the data line to the bit line.

36. A semiconductor memory device according to claim 1, further comprising a sense amplifier including a bit line and a write bit line for transferring data to and from the memory cell, a data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, data write means activated by a write signal for transferring data from the inverted write data line to the write bit line, precharge

means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line.

37. A semiconductor memory device according to claim 3, further comprising a sense amplifier including a write bit line connected to the read bit line for transferring data to and from the memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input connected to the read bit line, data read means for transferring an output of the inverter circuit to the read data line, data write means activated by the write signal for transferring data from the inverted write data line to the write bit line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line.

38. A semiconductor memory device according to claim 1, further comprising a sense amplifier including a bit line and a write bit line for transferring data to and from the memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line, wherein the write bit line is serially connected to the inverted write data line.

39. A semiconductor memory device according to claim 3, further comprising a sense amplifier including a write bit line connected to the read bit line for transferring data to and from a memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, precharge means for precharging the bit line, and level-maintaining means input with the output of

the inverter circuit for maintaining a level of the bit line, wherein the write bit line is serially connected to the inverted write data line.

40. A semiconductor memory device according to claim 1, further comprising a sub word driver selecting a read word line in response to a read block selection signal and an inverted read block selection signal and selecting a write word line in response to a main word signal, a write block selection signal and an inverted write block selection signal.

41. A semiconductor memory device according to claim 3, further comprising a sub word driver selecting a read word line in response to a read block selection signal and an inverted read block selection signal and selecting a write word line in response to a main word signal, a write block selection signal and an inverted write block selection signal.

42. A semiconductor memory device according to claim 1, comprising elements forming the memory cell placed in layout in an L-shaped region.

43. A semiconductor memory device according to claim 3, comprising elements forming the memory cell placed in layout in an L-shaped region.